REMARKS

The Examiner rejected claims 15-17, 19, 21-24, 26-28, 30-38 and 40-44 under 35 U.S.C. §102(e) as allegedly being anticipated by LaFollette et al. 6,610,440.

The Examiner rejected claims 18, 20, 25, 29 and 39 under 35 U.S.C. §103(a) as allegedly being unpatentable over LaFollette et al. 6,610,440 as applied to claims 15-17, 19, 21-24, 26-28, 30-38 and 40-43 above, and further in view of Bates et al. 5,561,004 and Wolk et al. 2001/0000744, previously applied.

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

35 U.S.C. §102(e)

The Examiner rejected claims 15-17, 19, 21-24, 26-28, 30-38 and 40-44 under 35 U.S.C. §102(e) as allegedly being anticipated by LaFollette et al. 6,610,440.

Applicants respectfully contend that LaFollette does not anticipate claim 15, because LaFollette does not teach each and every feature of claim 15.

As a first example why LaFollette does not anticipate claim 15, LaFollette does not teach the feature: "forming a layer of electronic devices on the semiconductor wafer, **wherein the layer of electronic devices includes at least one electronic device**" (emphasis added).

Although the Examiner alleges that layer 30 in LaFollette is a layer of electronic devices, Applicants contend that LaFollette discloses layer 30 to be of layer of silicon dioxide which is not a layer of electronic devices as required by claim 15. See LaFollette, FIG. 3 in which layer 30 is identified to be a layer of silicon dioxide. Applicants additionally contend that the Examiner's citation of col. 20, lines 15+ of LaFollette is not persuasive, because col. 20, lines 15+ of LaFollette does not disclose that layer 30 includes any electronic device.

In "Response to Arguments", the Examiner argues: "LaFollette clearly teaches at col. 12, lines 58-65, forming integrate circuit (IC, electronic device), MEMS and batteries on the same device". In response, Applicants note that FIGS. 4-5 of LaFollette show that system component 59' (IC, MEMS, etc.) is not included within layer 30 as alleged by the Examiner, but is instead on top of the polyimide spacer 38" which is in turn on top of the layer 30.

Moreover, Applicants maintain that none of the Examiner's cited references to LaFollette show that the layer 30 inherently includes an electronic device.

The Examiner's allegation that "any semiconductor textbook, such as Wolf" would teach that layer 30 could contain an electronic device is not persuasive, because the Examiner cannot combine a second reference (e.g., a semiconductor textbook) with LaFollette in a rejection under 35 U.S.C. §102(e).

Therefore, Applicants respectfully contend that the preceding feature of claim 15 does not read on LaFollette.

As a second example why LaFollette does not anticipate claim 15, LaFollette does not teach the feature: "forming a first conductive **metallization** and a second conductive **metallization** within the N wiring levels" (emphasis added).

The Examiner alleges that in LaFollette: the first conductive metallization is represented by interconnect 46, and the second conductive metallization is represented by interconnect 47 or 49. However, LaFollette does not explicitly teach that any of interconnects 46, 47, and 49 comprise metal. Therefore, Applicants respectfully contend that LaFollette does not explicitly teach that any of interconnects 46, 47, and 49 comprise conductive **metallization**.

Furthermore, Applicants respectfully contend that LaFollette does not inherently teach that any of interconnects 46, 47, and 49 comprise conductive **metallization**, since the interconnects 46, 47, and 49 does not have to include metal and may comprise a non-metallic electrically conductive material such as a electrically conductive semiconductor material. As an example, United States Patent U.S.P. 5,923,585 to Roberts et al. demonstrates the use of a polysilicon interconnect to effectuate electrically conductive coupling.

Therefore, Applicants respectfully contend that the preceding feature of claim 15 does

not read on LaFollette.

As a third example why LaFollette does not anticipate claim 15, LaFollette does not teach the feature: "forming at least one battery **within the wiring levels I through K**, wherein I is selected from the group consisting of 1, 2, ..., and N, wherein K is selected from the group consisting of I, I+1, ..., and N" (emphasis added).

Applicants respectfully contend that the wiring level having the maximum possible value of K in FIGS. 3-6 of LaFollette is the wiring level comprising the interconnect 47 or 49. Applicants maintain that the polymeric sealant 43' is not a wiring level.

However, the second microscopic electrode 48 of the battery 44' in FIGS. 3-6 of LaFollette is higher than the interconnect 47 or 49 (relative to the silicon substrate 32) and is therefore outside of the range of wiring levels I through K. Although the electrolyte 42' and the first microscopic electrode 34" of the battery 44' are within the range of wiring levels I through K, the electrolyte 42' and the first microscopic electrode 34" is not a battery. Thus the battery 44', which must include the second microscopic electrode 48, is not within the range of wiring levels I through K.

Therefore, Applicants respectfully contend that the preceding feature of claim 15 does not read on LaFollette.

Based on the preceding arguments, Applicants respectfully maintain that LaFollette does not anticipate claim 15, and that claim 15 is in condition for allowance. Since claims 16-17, 19, 21-24, 26, 26-28, 30-38, 40, and 42-43 depend from claim 15, Applicants contend that claims 16-

17, 19, 21-24, 26, 26-28, 30-38, 40, and 42-43 are likewise in condition for allowance.

In addition, LaFollette does not teach features specific to the dependent claims.

As a first example, LaFollette does not teach the following feature of claim 16: "polishing off top portions of the electrolyte layer and the second conductive material resulting in a planarized top surface of the electrolyte layer and the second conductive material, wherein a U-battery has been formed from the first conductive layer as the first electrode, the electrolyte layer as an electrolyte, and the second conductive material as the second electrode".

As a second example, LaFollette does not teach the following feature of claim 23: "polishing off top portions of the second conductive material, of the electrolyte layer, and of the first conductive layer, which results in a planarized top surface of the ILD layer, of the first conductive layer, of the electrolyte layer, and of the second conductive material, wherein a conductive contact is formed on the planarized top surface, wherein the conductive contact is in conductive contact with the second conductive material, wherein the first conductive metallization includes the conductive plate, and wherein the second conductive metallization includes the conductive contact, and wherein a U-battery With Double Extension has been formed from the first conductive layer as the first electrode, the electrolyte layer as an electrolyte, and the second conductive material as the second electrode".

As a third example, LaFollette does not teach the following feature of claim 27: "forming a second conductive layer on the electrolyte layer, wherein the second conductive layer includes a second conductive material, wherein the first conductive metallization includes the first conductive plate, and wherein a S-battery has been formed from the first conductive layer as the

first electrode, the electrolyte layer as an electrolyte, and the second conductive layer as the second electrode".

As a fourth example, LaFollette does not teach the following feature of claim 43: "wherein the step of forming a layer of electronic devices includes forming the layer of electronic devices during a Front-End-Of-Line (FEOL) processing of the integrated circuit, wherein the step of forming N wiring levels includes forming the N wiring levels during a Back-End-Of-Line (BEOL) integration of the integrated circuit, wherein the step of forming a first conductive metallization and a second conductive metallization includes forming the first conductive metallization and the second conductive metallization during the BEOL integration of the integrated circuit, and wherein the step of forming at least one battery includes forming the at least one battery during the BEOL integration of the integrated circuit".

35 U.S.C. §103(a)

The Examiner rejected claims 18, 20, 25, 29, and 39 under 35 U.S.C. §103(a) as allegedly being unpatentable over LaFollette et al. 6,610,440 in view of Bates et al. 5,561,004 and Wolk et al.

Since claims 18, 20, 25, 29, and 39 depend from claim 15, which Applicants have argued *supra* to not be unpatentable over LaFollette under 35 U.S.C. §102(e), Applicants maintain that claims 18, 20, 25, 29, and 39 are likewise not unpatentable over LaFollette in view of Bates and Wolk under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Date: 05/12/2005

Jack P. Friedman
Registration No. 44,688

Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110
(518) 220-1850